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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,319	11/26/2001	Tatsuya Takahashi	81784.0246	9511

7590 11/22/2005

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EXAMINER	
AGGARWAL, YOGESH K	
ART UNIT	**PAPER NUMBER**
2615	

DATE MAILED: 11/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 09/995,319	**Applicant(s)** TAKAHASHI, TATSUYA	
	Examiner Yogesh K. Aggarwal	**Art Unit** 2615	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 09 November 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: 1-12 and 16-20.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See attached sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☐ Other: _____.

DAVID L. OMETZ
SUPERVISORY PATENT EXAMINER

Examiner's response:

1. Applicant argues that Kothari does not teach "source follower amplification circuit". The Examiner respectfully disagrees. Transistors (M1A, M1B, M2A, M2B) amplify an input voltage (Vinput) and outputs an amplified voltage (Voutput), wherein the devices M1A and M1B share a common current source VDD2 (col. 3 line 56 – col. 4 line 9) and therefore acts as source follower amplification circuit. Furthermore, In response to applicant's arguments, the recitation source follower amplification circuit has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

2. Applicant argues with regards to claim 1 that there is no current flowing from Vdd2 to Vdd1. The Examiner respectfully disagrees. The claim recites "a load transistor connected between the amplification transistor and a first power source for **causing a constant current to flow** from the amplification transistor to the side of the first power source; a control transistor connected between the amplification transistor and a second power source, wherein the control transistor **controls a current flowing** from the second power source to the amplification transistor according to a control signal". Therefore according to the claim, a constant current flows from an amplification transistor to a first power source and **a current** flows from second power source to the amplification transistor. The claimed limitation **a current flowing** never refers back to the previously recited **a constant current.** In other words, the claim does not

require the two currents to be the same. Therefore as broadly as claimed, the prior art meets the recited limitations.

3. Applicant argues that Kothari does not teach "an output control circuit is connected to a gate of the control transistor for outputting the control signal for reducing a current flowing from the second power source to the amplification transistor during a period in which a pixel signal is not read". The Examiner respectfully disagrees. An output control circuit is shown in figure 2 as shift register and logic circuitry 24 is connected to a gate of the control transistor M9A and M9B through control signals phiPIX and phiNPIX (figure 3) for outputting the control signal for reducing a current flowing from the second power source to the amplification transistor during a period in which a pixel signal is not read (col. 5 line 46-col. 6 line 39, col. 1 lines 38-48). As clearly taught in Kothari at col. 5 line 66-col. 6 line 20, when the amplifier 33 is deselected, devices M9A and M9B (control transistors) are turned off during the pixel non-readout period, phiNPIX is high ,Vbias is grounded and current in self-biasing portion of the amplifier must have any residual current therein eliminated. Kothari further explains that when phiNPIX is high, transistor M14 in area 52 is activated thereby shutting-off all n-devices M7A, M8A, M7B, M8B and causes any current in transistors M5A-M8A and M5B-M8B to be grounded out (col. 6 lines 21-39). Therefore there is no current that flows from second power source (Vdd1) to the amplifier transistor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

4. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

5. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
November 16, 2005

DAVID L. OMETZ
SUPERVISORY PATENT
EXAMINER